

REMARKS

Claim 1 has been amended in order to broaden its scope. Claim 60 is a new claim dependent upon Claim 1. Claim 60 states that the indication is the native program counter value.

Claims 10-15 and 35-36 have been canceled to reduce the number of claims.

Claim 58 has been amended to make clear that when more than one bytecode is disposed at the same time, the JAVA PC is incremented in the correct manner.

Claims 1-9, 16-34 and 37-60 remain in the present application.

Respectfully submitted,

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Claims 1 and 58

1.(Amended) A system comprising:
a pipelined central processing unit with associated native program counter ; and
a hardware accelerator operably connected to the central processing unit, the
hardware accelerator adapted to convert stack-based instructions into register-based
instructions native to the central processing unit, the hardware accelerator including a reissue
buffer, the reissue buffer adapted to store converted native instructions issued to the CPU
along with [associated native program counter values] an indication of the order of the
instructions , the system is such that when the CPU returns from an interrupt, the reissue
buffer examines the [program counter value] indication to determine whether to reissue a
stored native instruction value.

58. (Amended) A system comprising:
a central processing unit with associated register file; and
a hardware accelerator operably connected to the central processing unit, the
hardware accelerator adapted to convert stack-based instructions into register-based
instructions native to the central processing unit, where the hardware accelerator increments
the Java PC within the hardware accelerator by generating an increment value based on the
number of byte codes being disposed, wherein the Java PC is incremented in the correct
manner if multiple bytecodes are disposed at the same time .